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10/609,216	06/26/2003	Karl H. Mauritz	42P16326	6486

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,216	MAURITZ ET AL.	
	Examiner	Art Unit	
	HETUL PATEL	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the BPAI decision mailed on 12/08/2008. The previous 112, 1st rejection of claims 1-30 is withdrawn and the prosecution on the merits of this application is reopened. Hence, this office action is made Non-final.

2. Claims 1-30 are currently pending in this application.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 7-8, 14, 17 and 19-21 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Karlquist (USPN: 2004/0202267)

As per claim 1, Morris teaches a circuit (i.e. 200 in Fig. 2) comprising: a plurality of memory modules (i.e. 201 in Fig. 2); a memory controller (i.e. 207 in Fig. 2) coupled

to the plurality of memory modules; and a plurality of terminators (i.e. 204, 210 in Fig. 2) to reduce signal reflections corresponding to the split signals (e.g. see Col. 4, 14-17 and Fig. 2). Morris also shows that the plurality of memory modules and the memory controller are connected via the memory board 203 and the system board 212 (see Fig. 2). Hence, there have to be some bus lines integrated on those boards (i.e. 203 and 212) for connecting/communicating the plurality of memory modules and the memory controller. However, Morris does not clearly disclose whether (i) a resistive bus splitter coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller (as claimed in the current application); or (ii) the same bus line connect in parallel to all memory modules (as alleged by Applicant in the remarks). If Applicant agrees with Morris interpretation as (i), then claim 1 is anticipated by Morris. If Applicant disagrees with Morris interpretation as (i) but agrees with (ii) (as recited in Remarks filed on 02/21/2008), then claim 1 is still unpatentable as being obvious over Karlquist. Karlquist teaches a resistive bus splitter (i.e. 205 in Fig. 2) to provide two separate circuit paths for splitting signals between two different components (i.e. 206 and 207 in Fig. 2) connected on the bus (see Fig. 2 and paragraph [0015]; Fig. 4 and paragraphs [0019]-[0020] also describes a 4-way resistive bus splitter (401)). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include a resistive bus splitter as taught by Karlquist between the plurality of memory modules and the memory controller taught by Morris to split signals

communicated between the plurality of memory modules and the memory controller. In doing so, the possible signal degradation is avoided.

As per claim 4, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above and furthermore, Morris teaches that the memory modules (i.e. 201 in Fig. 2) are dual in-line memory modules (DIMMs) (e.g. see Col. 3, lines 46-47 and Fig. 2).

As per claim 7, as described above in rejection of claim 1, the plurality of memory modules and the memory controller are connected via the memory board 203 and the system board 212 (see Fig. 2 of Morris). Hence, there have to be some bus lines integrated on those boards (i.e. 203 and 212) for connecting/communicating the plurality of memory modules and the memory controller.

As per claim 8, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above and furthermore, Morris teaches a plurality of memory expander chips (MXCs) (i.e. 201-1 and 201-2 in Fig. 3) coupled between the resistive bus splitter (i.e. embedded in 203 in Fig. 2) and the plurality of memory modules (i.e. 201 in Fig. 2) (e.g. see Fig. 2).

As per claims 14, 17 and 20-21, see arguments with respect to the rejection of claims 1, 4 and 7-8, respectively. Claims 14, 17 and 20-21 are also rejected based on the same rationale as the rejection of claims 1, 4 and 7-8, respectively.

As per claim 19, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above and furthermore, Morris teaches that the resistive bus splitter includes a miniature resistive splitter on a PCB (i.e. a plurality of

resistors in order to reduce the noise in the signals sent to DIMMs are *inherently embedded* on the memory board 203 in Fig. 2 of Morris) (e.g. see Fig. 2 of Morris). Karlquist also discloses the resistive bus splitter includes a miniature resistive splitter on a PCB (see 205 and 401 in Figs. 2 and 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-3 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over (i) Morris or, in the alternative, (ii) the combination of Morris and Karlquist.

As per claims 2 and 3, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above and furthermore, Morris teaches that the plurality of terminators (i.e. 204, 210 in Fig. 2) are attached/mounted on the memory board 203 in Fig. 2. Official notice is taken of the prior art teaching a plurality of components (i.e. terminators) on a single chip. First of all, it has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965). Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure would be obvious. Integrating/embedding multiple components on a single chip reduces cabling problems, reduces latency required for communicating among

processors, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple terminators embedded on the memory module/memory controller provides improvements in efficiency, cost and scalability over terminators mounted on a circuit board(s), it would have been obvious to use a single chip design in the device of Morris. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

As per claims 15-16, see arguments with respect to the rejection of claims 2 and 3, respectively. Claims 15-16 are also rejected based on the same rationale as the rejection of claims 2 and 3, respectively.

5. Claims 8-13 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over (i) Morris in view of Talbot et al. (USPN: 2005/0166006) hereinafter, Talbot or, in the alternative, (ii) Morris in view of Karlquist and Talbot.

As per claim 8, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above and furthermore, Morris teaches a plurality of memory expander chips (MXCs) (i.e. 201-1 and 201-2 in Fig. 3) coupled between the memory controller (i.e. 207 in Figs. 2-3) and the plurality of memory modules. Suppose even if Morris does not specifically define 201-1 and 201-2 in Fig. 3 as a plurality of memory expander *chips* (MXCs) as claimed, Talbot, on the other hand, teaches a plurality of memory expander chips (MXCs) (i.e. the memory control hubs

160A-160B in Fig. 1) coupled between the memory controller (i.e. 106 in Fig. 1) and the plurality of memory modules (i.e. 171A-171N in Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include a plurality of memory expander chips taught by Talbot in the circuit taught by Morris (or alternatively the combination of Morris and Karlquist). In doing so, a large number of memory modules can be connected to the circuit. Therefore, it is being advantageous. Furthermore, in doing so, address signals are sent through a plurality of MXCs between the resistive bus splitter and the plurality of memory modules.

As per claim 9, the combination of Morris and Talbot (or alternatively the combination of Morris, Karlquist and Talbot) teaches the claimed invention as described above and furthermore, Talbot teaches that the plurality of MXCs (i.e. 160A-160B in Fig. 1) enable access to relative larger memory arrays (i.e. 171A-171N and 181A-181N in Fig. 1).

As per claim 10, the combination of Morris and Talbot (or alternatively the combination of Morris, Karlquist and Talbot) teaches the claimed invention as described above and furthermore, Talbot teaches that each of the plurality of MXCs (i.e. 160A-160B in Fig. 1) include a built in bi-directional cache (i.e. the cache 175A, 175B in Fig. 1) to decrease latency and increase throughput efficiency (e.g. see Fig. 1).

As per claim 11, the combination of Morris and Talbot (or alternatively the combination of Morris, Karlquist and Talbot) teaches the claimed invention as described above. The further limitation, of having a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported

DIMMs, is also *inherently* taught by Talbot because by coupling a MXC (i.e. 201-1 in Fig. 3) between a plurality (i.e. two) of memory modules/DIMMs (i.e. 201 in Fig. 2), the bandwidth gets doubled compared to if a DIMM is directly connected to the controller (i.e. 207 in Figs. 2-3) (e.g. see Figs. 2-3).

As per claim 12, the combination of Morris and Talbot (or alternatively the combination of Morris, Karlquist and Talbot) teaches the claimed invention as described above and furthermore, Talbot teaches about having access coalescing functionality (i.e. access uniting) in each of the plurality of MXCs (i.e. 160A and 160B in Fig. 1). For example, accesses from a plurality of memory chips (i.e. 171A-171N in Fig. 1) are coalesced/gathered by the hub 160 A (e.g. see Fig. 1).

As per claim 13, the combination of Morris and Talbot (or alternatively the combination of Morris, Karlquist and Talbot) teaches the claimed invention as described above and furthermore, Talbot teaches that a portion of the plurality of MXCs (i.e. 160A-160B in Fig. 1) are coupled to each other in series (e.g. see Fig. 1).

As per claims 21-26, see arguments with respect to the rejection of claims 8-13, respectively. Claims 21-26 are also rejected based on the same rationale as the rejection of claims 8-13, respectively.

6. Claims 5-6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over (i) Morris in view of Jeddeloh et al. (USPN: 2004/0044933) hereinafter, Jeddeloh or, in the alternative, (ii) Morris in view of Karlquist and Jeddeloh.

As per claim 5, Morris (or alternatively the combination of Morris and Karlquist) teaches the claimed invention as described above, but Morris failed to teach that the circuit further including a reference voltage generator to generate a reference voltage corresponding to a memory chip voltage. Jeddeloh discloses a reference voltage generator (i.e. the combination of 74 and 76 in Fig. 2), which generates a reference voltage (i.e. V_{Ref}) corresponding to a memory chip voltage (e.g. see paragraph [0025] and Fig. 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the reference voltage generator taught by Jeddeloh in Morris's circuit. In doing so, the memory modules 60a, 60b may use the reference voltage Vref to determine data bit values during data sensing, writing and reading operations.

As per claim 6, the combination of Morris and Jeddeloh (or alternatively the combination of Morris, Karlquist and Jeddeloh) teaches the claimed invention as described above and furthermore, Jeddeloh teaches that the reference voltage (i.e. V_{Ref}) is provided to the plurality of memory modules (i.e. 60a and 60b in Fig. 2) and the memory controller (i.e. 100 in Fig. 2) (e.g. see paragraph [0025] and Fig. 2).

As per claims 18, see arguments with respect to the rejection of claims 5 and 6. Claim 18 is also rejected based on the same rationale as the rejection of claims 5 and 6.

7. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freker (USPN: 6,442,645) in view of Morris.

As per claim 27, Freker teaches a computer system (i.e. 100 in Fig. 1) comprising: a central processing unit (CPU) (i.e. the processor 105 in Fig. 1); a display device (i.e. 125 in Fig. 1) coupled to the CPU to display an image; a plurality of memory modules (i.e. the memory array 120 in Figs. 1-2); a memory controller (i.e. 116 in Fig. 2) coupled to the plurality of memory modules (i.e. $210_{1\text{-}4}$ in Fig. 2) and the CPU (e.g. see Figs. 1-2). However, Freker does not clearly disclose a plurality of bus splitters and a plurality of terminators. Morris, on the other hand, teaches a plurality of bus splitters coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller (i.e. embedded in the memory board 203 to split the signals sent from high speed connectors 205 and 209 into plurality of connectors 202 coupled to the memory modules 201 in Fig. 2); and a plurality of terminators (i.e. 204, 210 in Fig. 2) to reduce signal reflections corresponding to the split signals (e.g. see Col. 4, 14-17 and Fig. 2). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement a plurality of bus splitters and a plurality of terminators of Morris in the computer system taught by Freker. By implementing bus splitters, the signals from the memory controller can be split and then sent to a plurality of memory modules at the same time and by implementing terminators, signal reflections can be reduced or totally avoided. Therefore, it is being advantageous.

As per claim 28, the combination of Freker and Morris teaches the claimed invention as described above. The further limitation of selecting miniature integrated resistor packs as the resistive bus splitter is inherently taught by Morris. The miniature

integrated resistor packs has to be present in the memory board (i.e. 203 in Fig. 3A) in order to reduce the noise in the signals sent to DIMMs.

As per claim 29, the combination of Freker and Morris teaches the claimed invention as described above and furthermore, Morris teaches that the system further including a plurality of memory expander chips (i.e. 201-1 and 201-2 in Fig. 3) coupled between the resistive bus splitter (i.e. embedded in the memory board 203 to split the signals sent from high speed connectors 205 and 209 into plurality of connectors 202 coupled to the memory modules 201 in Fig. 2) and the plurality of memory modules (i.e. 201 in Fig. 2) to perform memory functions independent of the memory controller (i.e. 207 in Fig. 2) (e.g. see Figs. 2-3).

8. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freker (USPN: 6,442,645) in view of Morris, further in view of Nizar et al. (USPN: 6,889,284) hereinafter, Nizar.

As per claim 30, the combination of Freker and Morris teaches the claimed invention as described above. However, none of them teaches that the MXC functions include at least one of refresh, dynamic address space re-mapping and memory POST. Nizar, however, teaches that the MXC (i.e. the memory translator hub 100 in Fig. 1) functions include refresh operation (e.g. see claim 9 and Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the computer system taught by the combination of Freker and Morris as taught by Nizar so the MXC can perform the refresh operation on memory

modules. In doing so, the main controller (i.e. the processor 130 in Fig. 1) can be relieved from the burden of refreshing all the memory modules connected to it. Therefore, the overall performance of the computer system improves.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hetul Patel/
Patent Examiner
Art Unit 2186